

CLAIMS:

1. A method of selecting a signal among N signals, the selection taking place in that a validation signal associated with the signal to be selected is placed in an active state by means of a selection signal, which method includes an attribution step in which the state of the associated selection signal is attributed to each of the validation signals, which attribution
5 step is carried out when all the validation signals are in an inactive state.

2. A method of selecting a signal among N signals, the selection taking place in that a validation signal associated with the signal to be selected is placed in an active state by means of a selection signal, which method comprises a reset step in which those validation
10 signals which have not presented an active front since a given moment in time are reset to an inactive state, which reset step is carried out when at least two validation signals are simultaneously in an active state.

3. A method of selecting a signal among N signals, the selection taking place in that a validation signal associated with the signal to be selected is placed in an active state by means of a selection signal, which method includes a reset step in which all validation signals
15 which have not presented an active front since a given moment in time are reset to an inactive state, which reset step is carried out when one of the validation signals presents an active front.

4. A method of selecting a signal among N signals, the selection taking place in that a validation signal associated with the signal to be selected is placed in an active state by means of a selection signal, which method is characterized in that it comprises attribution and
20 reset steps as claimed in claims 1 to 3.

5. A method enabling a chip card to exchange data with a machine, wherein a clock signal selected among N clock signals supplied by the machine is transmitted to the chip card, which method is characterized in that it utilizes for this purpose a method as
25 claimed in one of the claims 1 to 4.

6. A switching device designed to deliver at an output a signal selected among N input signals when a validation signal associated with said input signal has been placed in an active state by means of an associated selection signal, which device includes:

- 5 - attribution means capable of attributing to each of the validation signals the state of its associated selection signal, which means are intended to be activated when all the validation signals are in an inactive state, and
- reset means capable of resetting to an inactive state those of the validation signals which have not presented an active front since a given moment in time, which means are
10 intended to be activated when at least two validation signals simultaneously have an active state.

7. A switching device as claimed in claim 6, ^{wherein} ~~characterized in that~~ it comprises in addition:

- 15 - detection means for detecting active fronts of the selection signals, and
- memory means for storing the state of the selection signals, which means are intended to be activated by the active fronts of said signals and to deliver the validation signals.

8. A switching device as claimed in claim 7, ^{wherein} ~~characterized in that~~ it comprises in addition:

- 20 - detection means for detecting that all the validation signals are simultaneously inactive, which detection means are intended to control the attribution means.

9. A switching device as claimed in claim 7, ^{wherein} ~~characterized in that~~ it comprises in addition:

- 25 - detection means for detecting active fronts of the validation signals, which detection means are intended to control the reset means.

10. An apparatus intended to exchange data with a smart card, and especially
30 supplying thereto a clock signal selected among N clock signals, which apparatus ~~is~~ ^{is} characterized in that it comprises a switching device as claimed in claim 6.